TCA9554A Low Voltage 8-Bit I²C and SMBus Low-Power I/O Expander With Interrupt Output and Configuration Registers

1 Features

- Low Standby Current Consumption
- I²C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I²C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I²C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (e.g. Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

3 Description

The TCA9554A is a 16-pin device that provides 8 bits of general purpose parallel input/output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V. The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA9554A provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

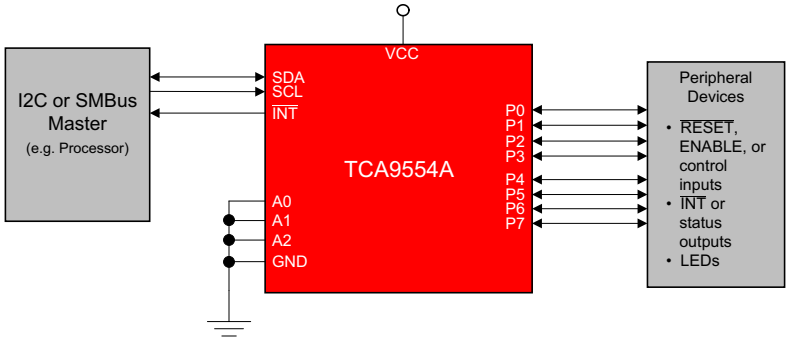
The features of the TCA9554A include an interrupt that is generated on the $\overline{INT}$ pin whenever an input port changes state. The A0, A1, and A2 hardware selectable address pins allow up to eight TCA9554A devices on the same I²C bus. The device can also be reset to its default sate by cycling the power supply and causing a power-on reset.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9554A	TSSOP (16)	5.00 mm × 4.40 mm
	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision A (March 2012) to Revision B **Page**

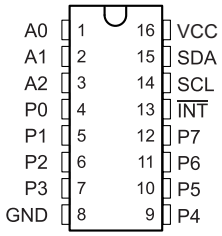
- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

Changes from Original (August 2014) to Revision A **Page**

- Initial release of full version ... 1
- Updated part number in the DESCRIPTION/ORDERING INFORMATION section. ... 12

6 Pin Configuration and Functions

PW OR DBQ PACKAGE
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
A0	1	Address input. Connect directly to V_{CC} or ground.
A1	2	Address input. Connect directly to V_{CC} or ground.
A2	3	Address input. Connect directly to V_{CC} or ground.
P0	4	P-port input/output. Push-pull design structure. At power on, P0 is configured as an input.
P1	5	P-port input/output. Push-pull design structure. At power on, P1 is configured as an input.
P2	6	P-port input/output. Push-pull design structure. At power on, P2 is configured as an input.
P3	7	P-port input/output. Push-pull design structure. At power on, P3 is configured as an input.
GND	8	Ground
P4	9	P-port input/output. Push-pull design structure. At power on, P4 is configured as an input.
P5	10	P-port input/output. Push-pull design structure. At power on, P5 is configured as an input.
P6	11	P-port input/output. Push-pull design structure. At power on, P6 is configured as an input.
P7	12	P-port input/output. Push-pull design structure. At power on, P7 is configured as an input.
$\overline{INT}$	13	Interrupt output. Connect to V_{CC} through a pull-up resistor.
SCL	14	Serial clock bus. Connect to V_{CC} through a pull-up resistor.
SDA	15	Serial data bus. Connect to V_{CC} through a pull-up resistor.
VCC	16	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current through a single P-port	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current through a single P-port	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND by all P-ports, $\overline{INT}$, and SDA			250	mA
	Continuous current through V_{CC} by all P-ports			–160	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	0.7 × V_{CC}	V_{CC}(1)	V
		A2–A0, P7–P0	V_{CC} = 1.65 V to 2.7 V	0.7 × V_{CC}	5.5	
			V_{CC} = 3.0 V to 5.5 V	0.8 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	–0.5	0.3 × V_{CC}	V
		A2–A0, P7–P0	V_{CC} = 1.65 V to 2.7 V	–0.5	0.3 × V_{CC}	
			V_{CC} = 3.0 V to 5.5 V	–0.5	0.2 × V_{CC}	
I_{OH}	High-level output current	Any P-port, P7–P0			–10	mA
I_{OL}	Low-level output current	Any P-port, P7–P0			25	mA
I_{CC}	Continuous current through GND	All P-ports P7-P0, $\overline{INT}$, and SDA			200	mA
	Continuous current through V_{CC}	All P-ports P7-P0			–80	
T_A	Operating free-air temperature			–40	85	°C

(1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V_{CC} in the application, or an increase in leakage current, I_I, will result.

7.4 Thermal Information

THERMAL METRIC(1)		TCA9554A		UNIT
		PW	DBQ	
		16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.0	121.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	72.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	64.2	
ψ_{JT}	Junction-to-top characterization parameter	10.8	24.4	
ψ_{JB}	Junction-to-board characterization parameter	66.5	63.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1.0		V

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		I_{OH} = –10 mA	1.65 V	1.1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4.0			
I_{OL}	SDA(3)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	11		mA
	P port(4)	V_{OL} = 0.5 V	1.65 V	8	10		
			2.3 V	8	13		
			3 V	8	15		
			4.5 V	8	17		
		V_{OL} = 0.7 V	1.65 V	10	14		
			2.3 V	10	17		
			3 V	10	20		
			4.5 V	10	24		
	$\overline{INT}$ (5)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	7		
I_I	SCL, SDA	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	1.65 V to 5.5 V			–100	µA
I_{CC}	Operating mode	V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{scl} = 400 kHz, No load t_r = 3 ns	5.5 V		18	30	µA
		V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{scl} = 400 kHz, No load $t_{r,max}$ = 300 ns	5.5 V		34		
			3.6 V		15		
			2.7 V		9		
			1.65		5		
		V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{scl} = 100 kHz $t_{r,max}$ = 1 µs	5.5 V		20		
			3.6 V		8		
			2.7 V		5		
			1.65 V		3		
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		450	700	
			3.6 V		300	600	
			2.7 V		225	500	
			1.95 V		225	500	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	1.65 V to 5.5 V			1.5	mA
C_i	SCL	V_I = V_{CC} or GND	1.65 V to 5.5 V		4	5	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	1.65 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V_{CC} should be limited to a maximum current of 80 mA.
(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND should be limited to a maximum current of 200 mA.
(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND should be limited to a maximum current of 200 mA.
(5) The $\overline{INT}$ pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND should be limited to a maximum current of 200 mA.

7.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 10)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	20	300	ns
t_{icf}	I²C input fall time			300	20 × (V_{DD} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	20 × (V_{DD} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45		0.9	ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45		0.9	µs
C_b	I²C bus capacitive load			400		400	pF

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 11 and Figure 12)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		350		350	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

7.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

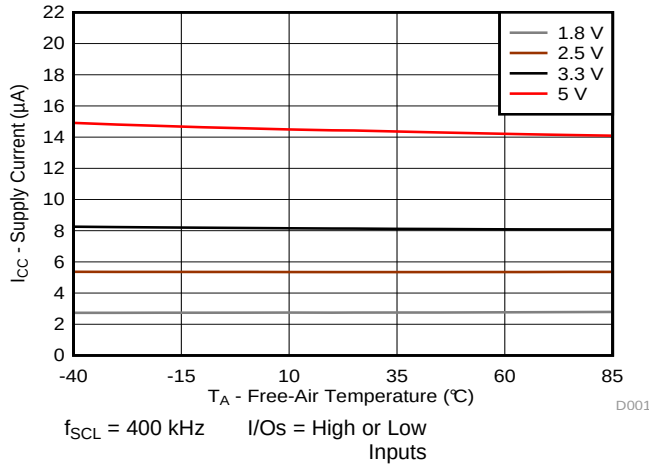


Figure 1. Supply Current (I_{CC}, Operating Mode) vs. Temperature (T_A) at Four Supply Voltages

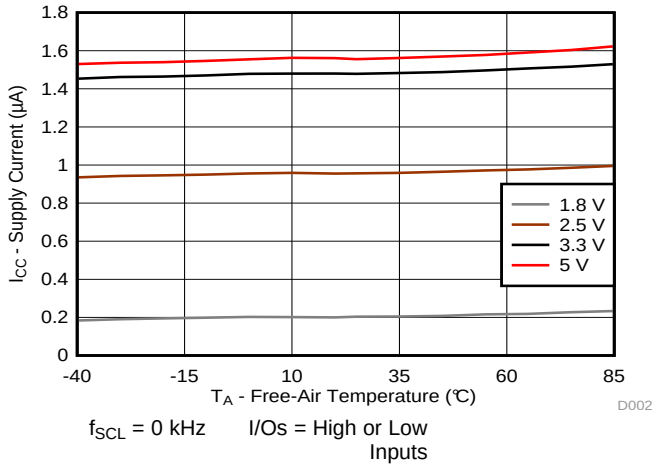


Figure 2. Supply Current (ICC, Standby Mode) vs. Temperature (T_A) at Four Supply Voltages

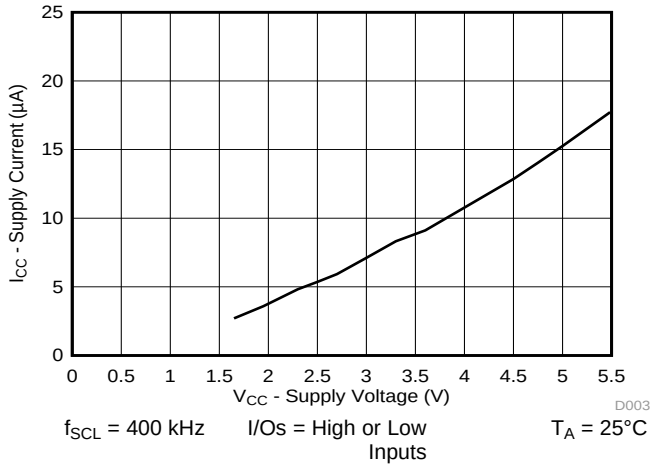


Figure 3. Supply Current (I_{CC}, Operating Mode) vs. Supply Voltage (V_{CC})

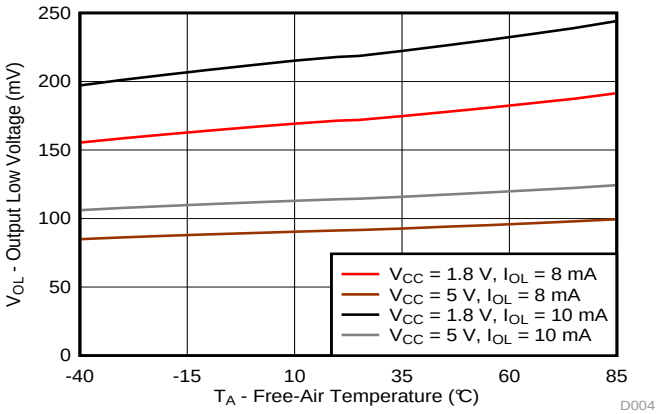


Figure 4. Output Low Voltage (V_{OL}) vs. Temperature (T_A) for P-Port I/Os

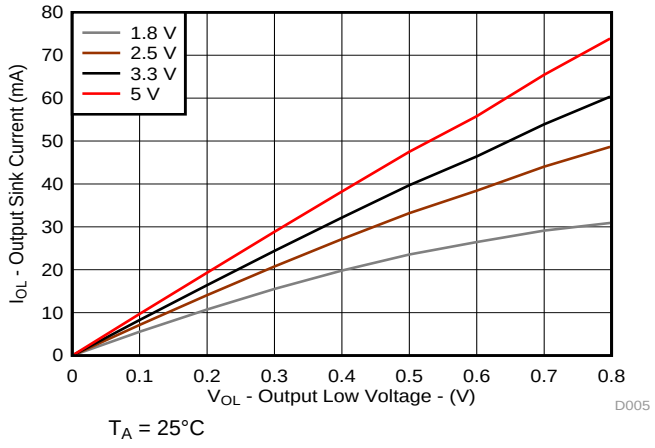


Figure 5. Sink Current (I_{OL}) vs. Output Low Voltage (V_{OL}) for P-Ports at Four Supply Voltages

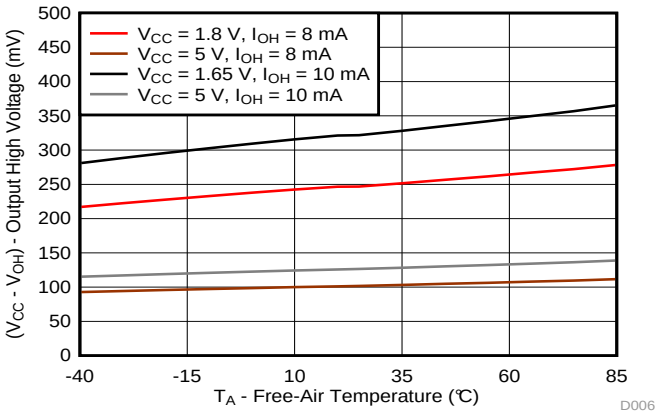


Figure 6. Output High Voltage (V_{CC} - V_{OH}) vs. Temperature (T_A) for P-Ports

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

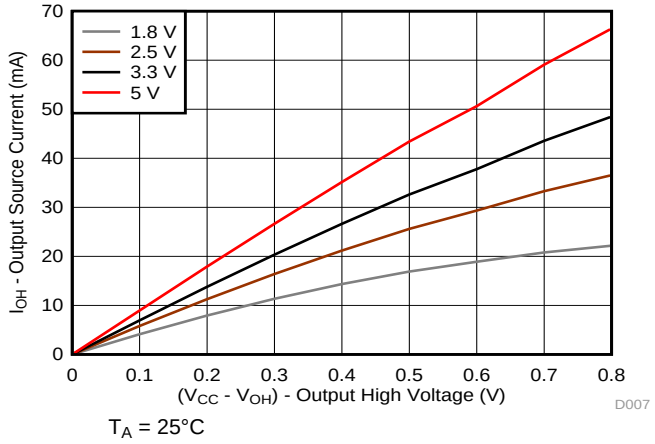


Figure 7. Source Current (I_{OH}) vs. Output High Voltage (V_{OH}) for P-Ports at Four Supply Voltages

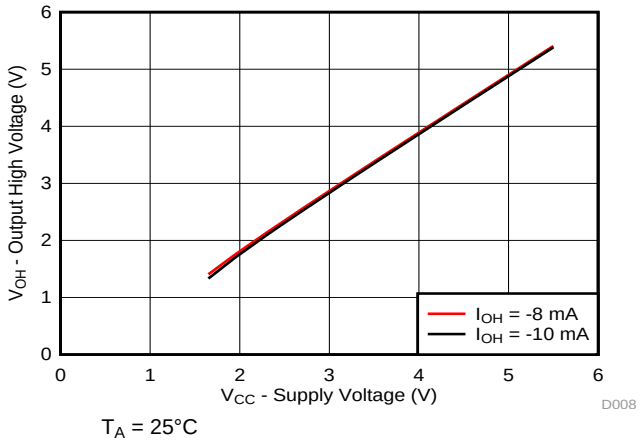


Figure 8. Output High Voltage (V_{OH}) vs. Supply Voltage (V_{CC}) for P-Ports

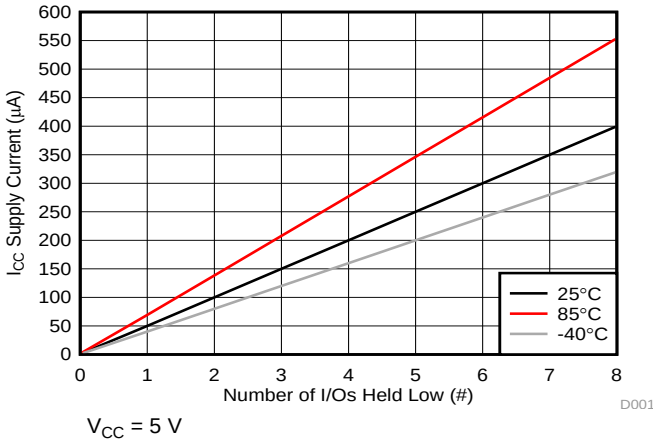
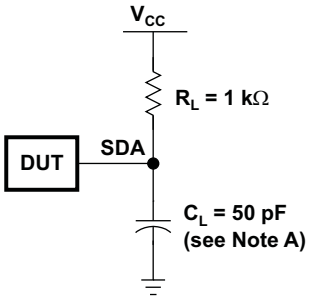
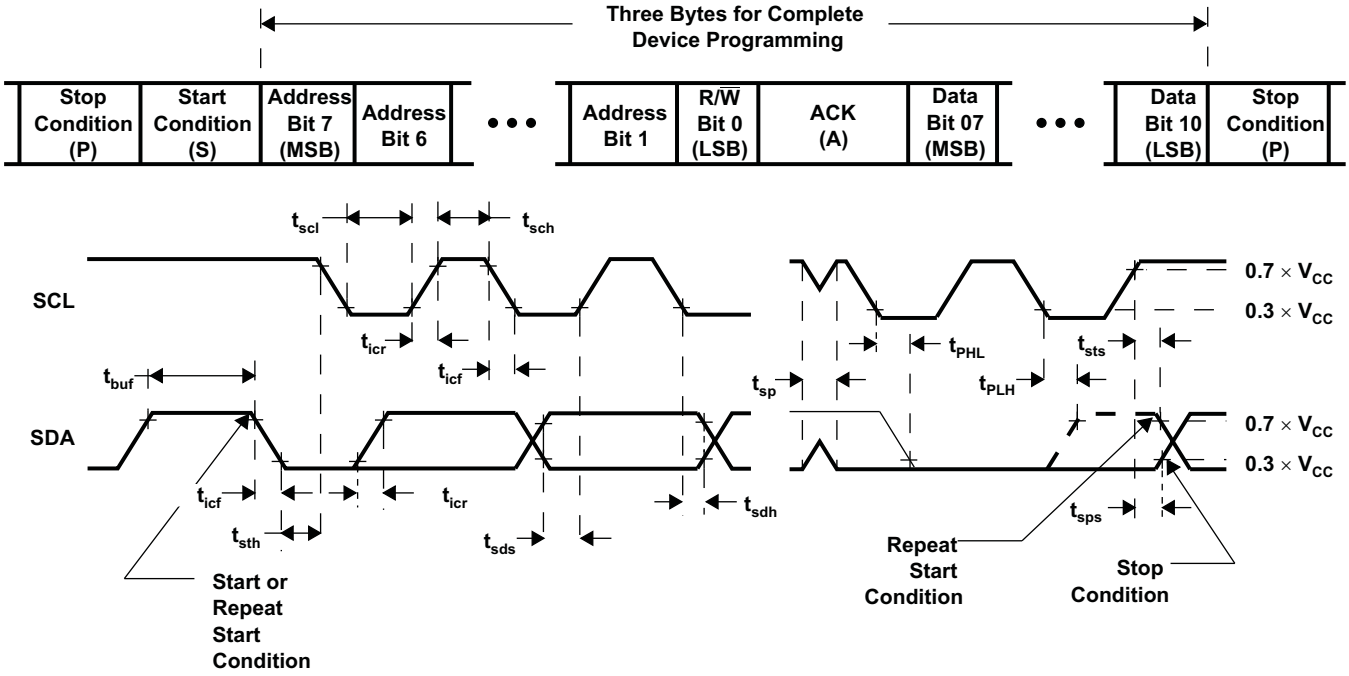


Figure 9. Supply Current (I_{CC}) vs. Number of I/Os Held Low (#)

8 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

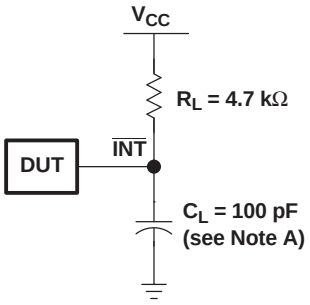
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

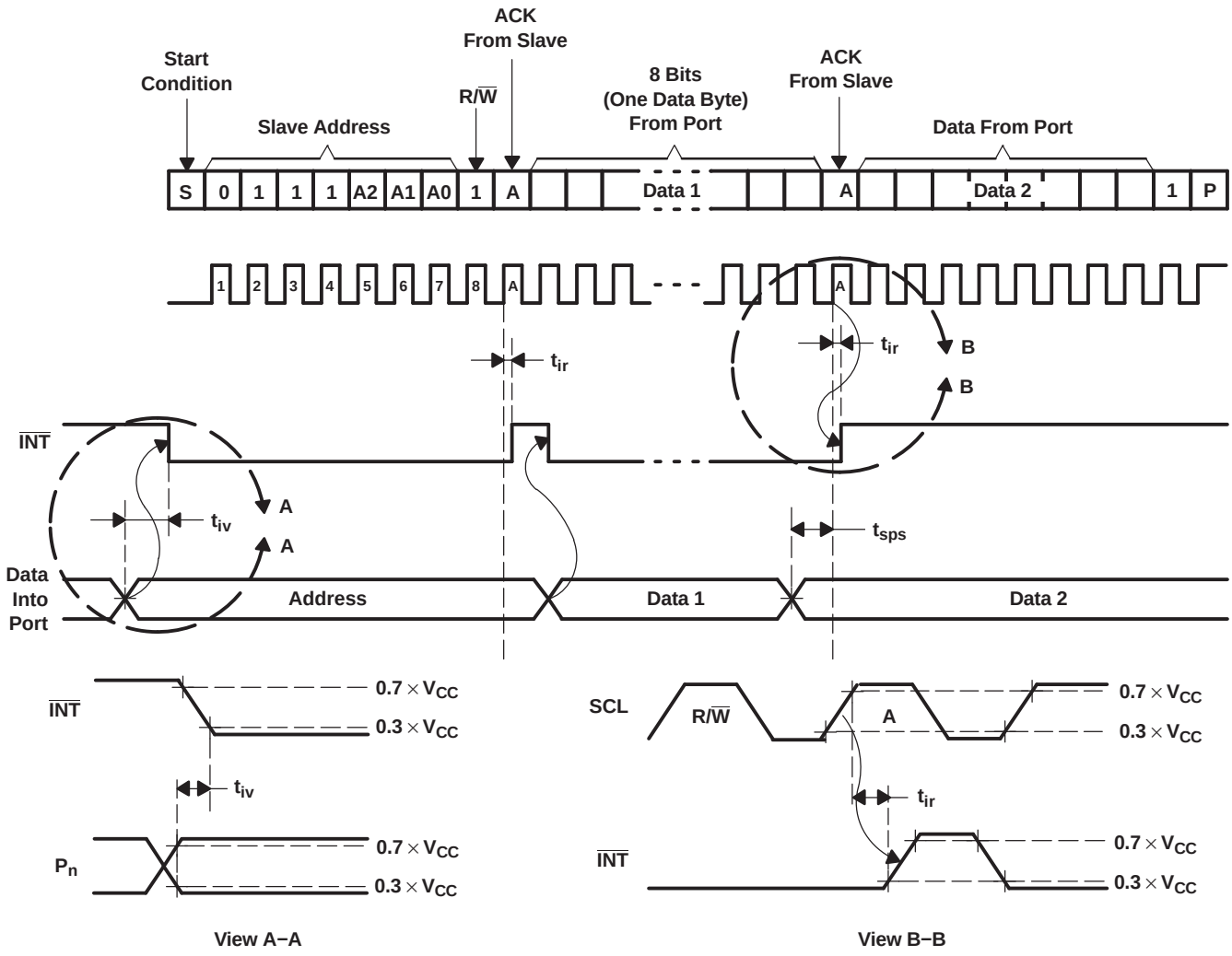
C. All parameters and waveforms are not applicable to all devices.

Figure 10. I^2C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



View A–A

View B–B

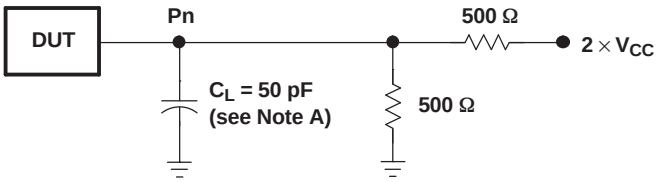
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

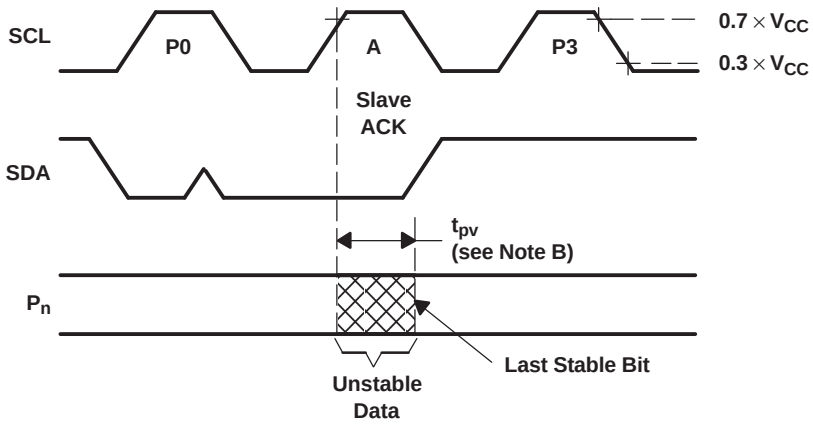
C. All parameters and waveforms are not applicable to all devices.

Figure 11. Interrupt Load Circuit And Voltage Waveforms

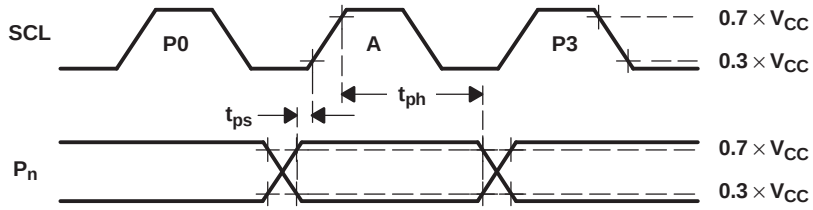
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 12. P-Port Load Circuit And Voltage Waveforms

9 Detailed Description

9.1 Overview

The TCA9554A is an 8-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I^2C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9554A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I2C bus. Thus, the TCA9554A can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C slave address and allow up to eight devices to share the same I^2C bus or SMBus.

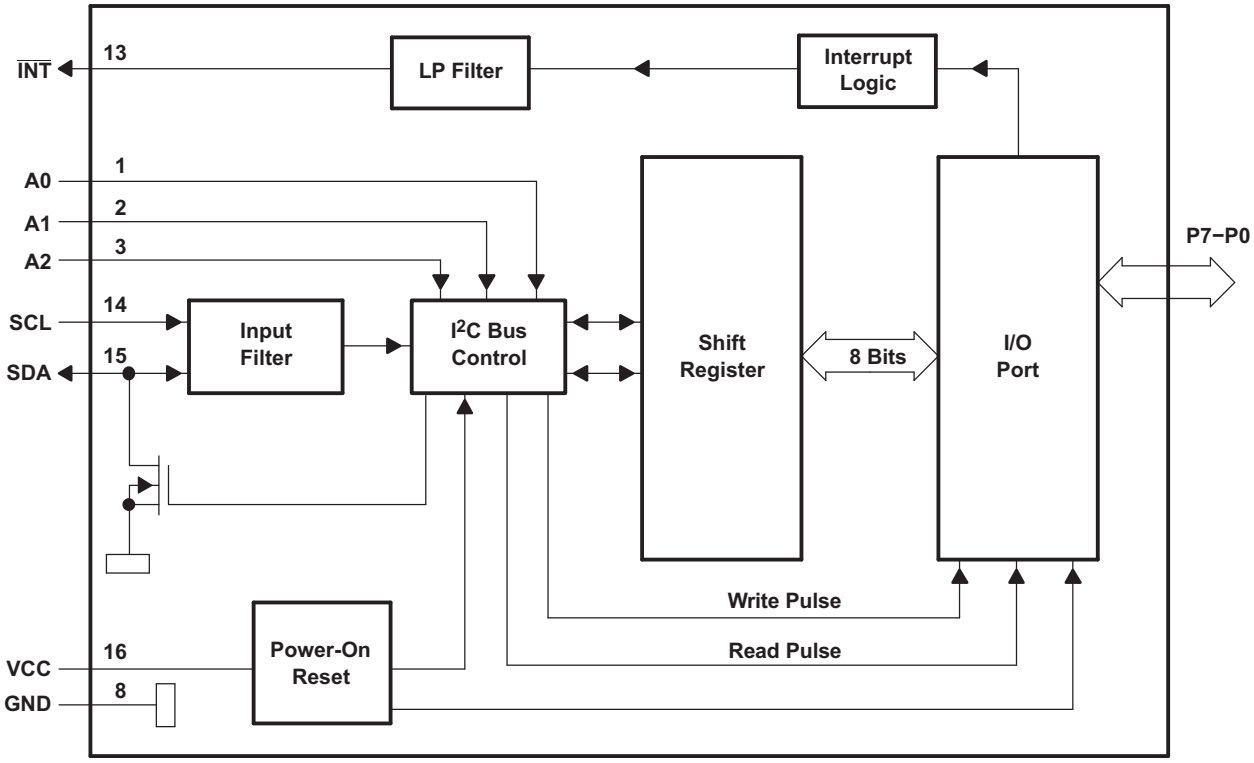
The system master can reset the TCA9554A in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I^2C /SMBus state machine.

The TCA9554A consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9554A and TCA9554 are identical except for their fixed I^2C address. This allows for up to 16 of these devices (8 of each) on the same I^2C/SMBus.

The TCA9554A is identical to the TCA9534A except for the addition of the internal I/O pull-up resistors, which keeps P-ports from floating when configured as inputs.

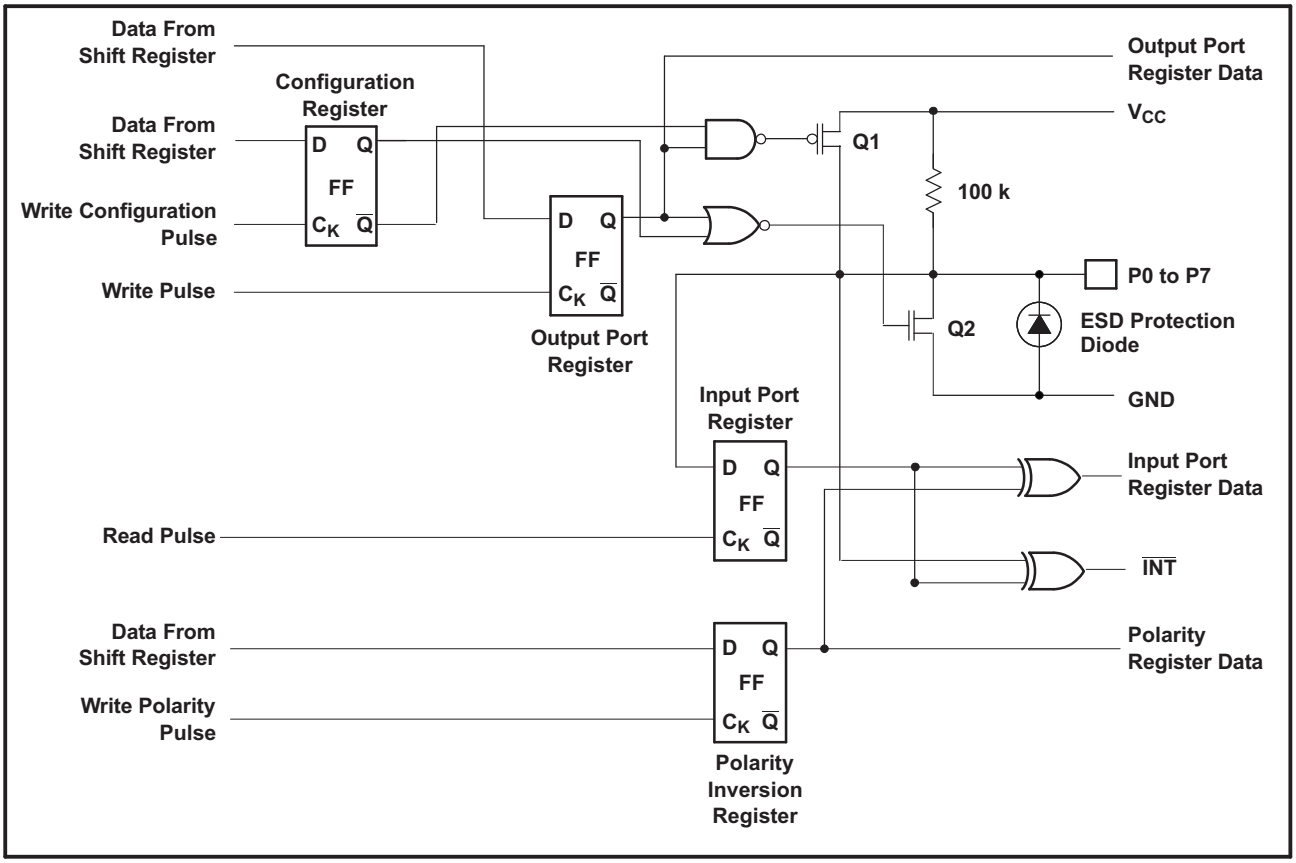
9.2 Functional Block Diagram



A. Pin numbers shown are for the PW package.

Figure 13. Functional Block Diagram

Functional Block Diagram (continued)



A. At power-on reset, all registers return to default values.

Figure 14. Simplified Schematic Of P0 To P7

9.3 Feature Description

9.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

9.3.2 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of any P-port I/O configured as an input. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the ports is changed back to the original state or when data is read from the Input Port register. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as an interrupt on the $\overline{INT}$ pin.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

9.4 Device Functional Modes

9.4.1 Power-On Reset

When power (from 0 V) is applied to VCC, an internal power-on reset holds the TCA9554A in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9554A registers and SMBus/I^2C state machine will initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and then back up to the operating voltage for a power-on reset cycle.

9.5 Programming

9.5.1 I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 15). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and the Stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 16).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 15).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 17). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

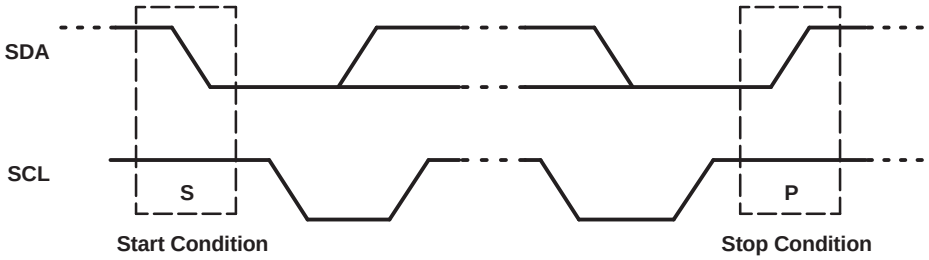


Figure 15. Definition of Start and Stop Conditions

Programming (continued)

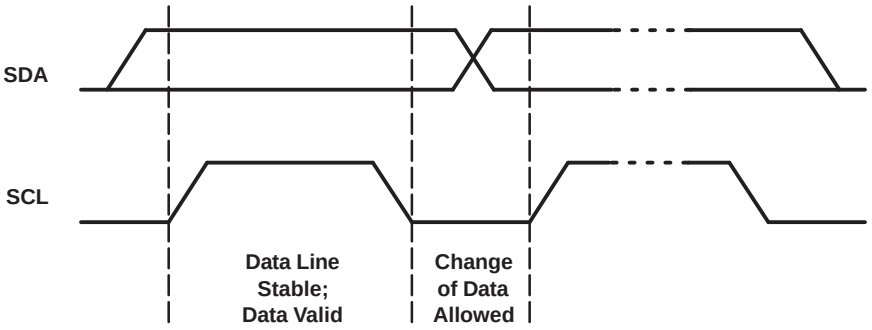


Figure 16. Bit Transfer

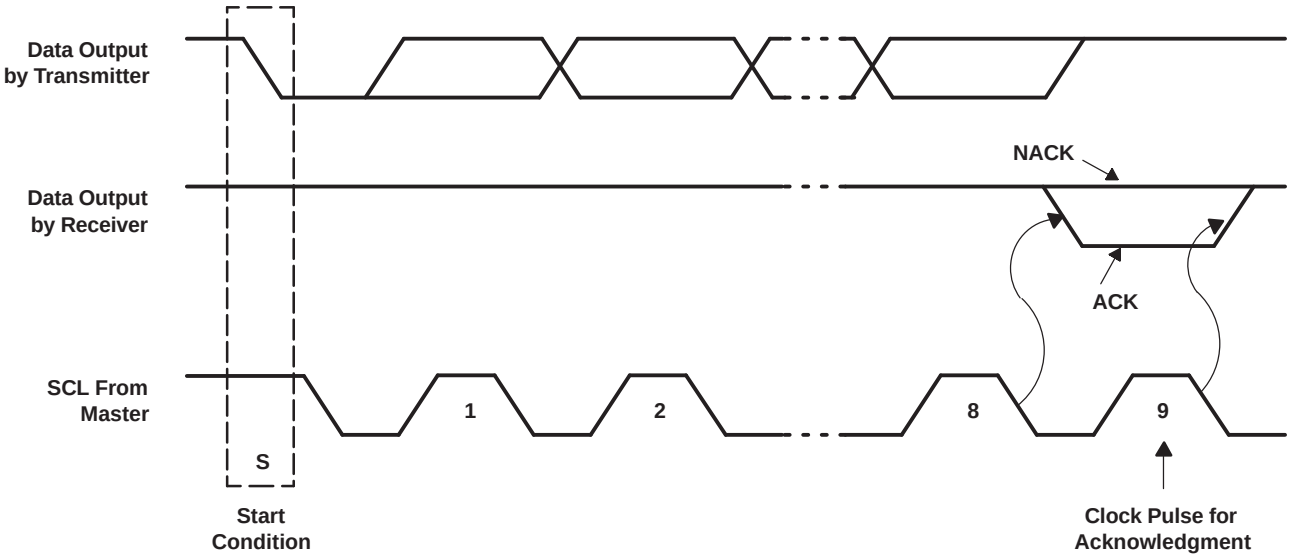


Figure 17. Acknowledgment on I^2C Bus

Table 1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	H	H	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

9.6 Register Map

9.6.1 Device Address

Figure 18 shows the address byte of the TCA9554A.

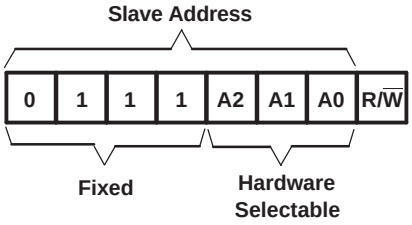


Figure 18. TCA9554A Address

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

9.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9554A (see Figure 19). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	0	B1	B0

Figure 19. Control Register Bits

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

9.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next.

Table 4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

Table 6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

9.6.3.1 Bus Transactions

Data is exchanged between the master and TCA9554A through write and read commands.

9.6.3.1.1 Writes

Data is transmitted to the TCA9554A by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 20 and Figure 21). There is no limitation on the number of data bytes sent in one write transmission.

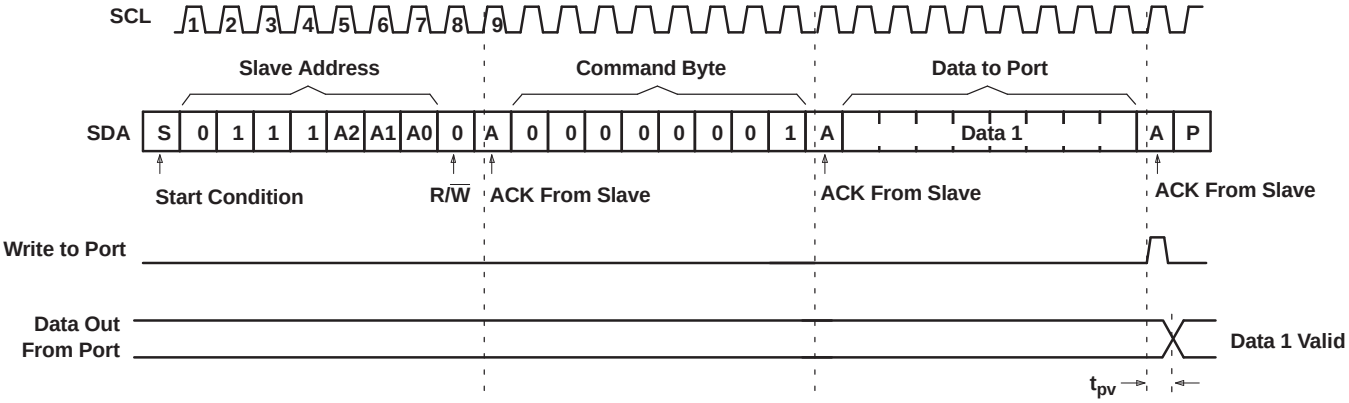


Figure 20. Write to Output Port Register

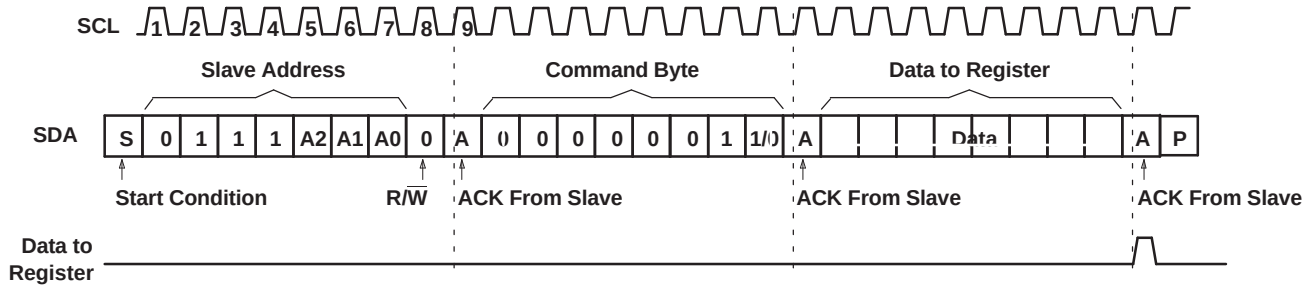


Figure 21. Write to Configuration or Polarity Inversion Registers

9.6.3.1.2 Reads

The bus master first must send the TCA9554A address with the LSB set to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9554A (see Figure 22 and Figure 23). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

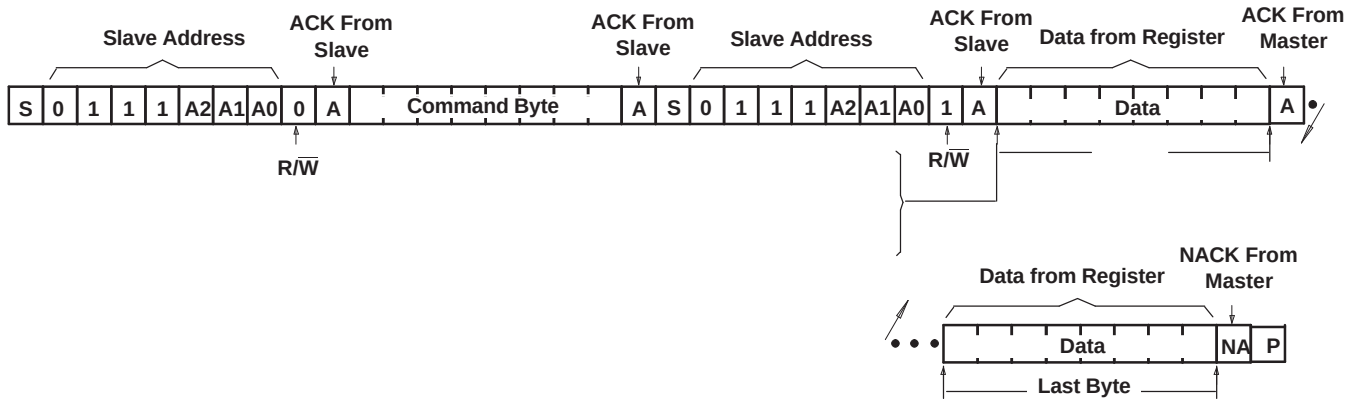
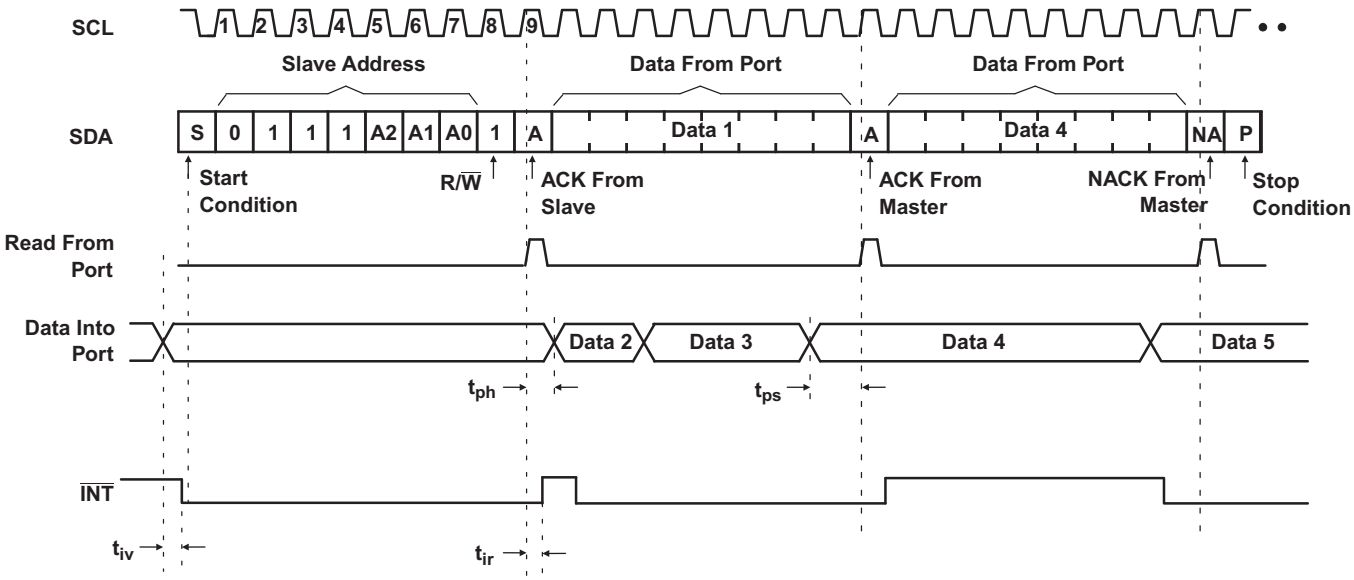


Figure 22. Read From Register



A. This figure assumes the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See Figure 22 for these details.

Figure 23. Read From Input Port Register

10 Application and Implementation

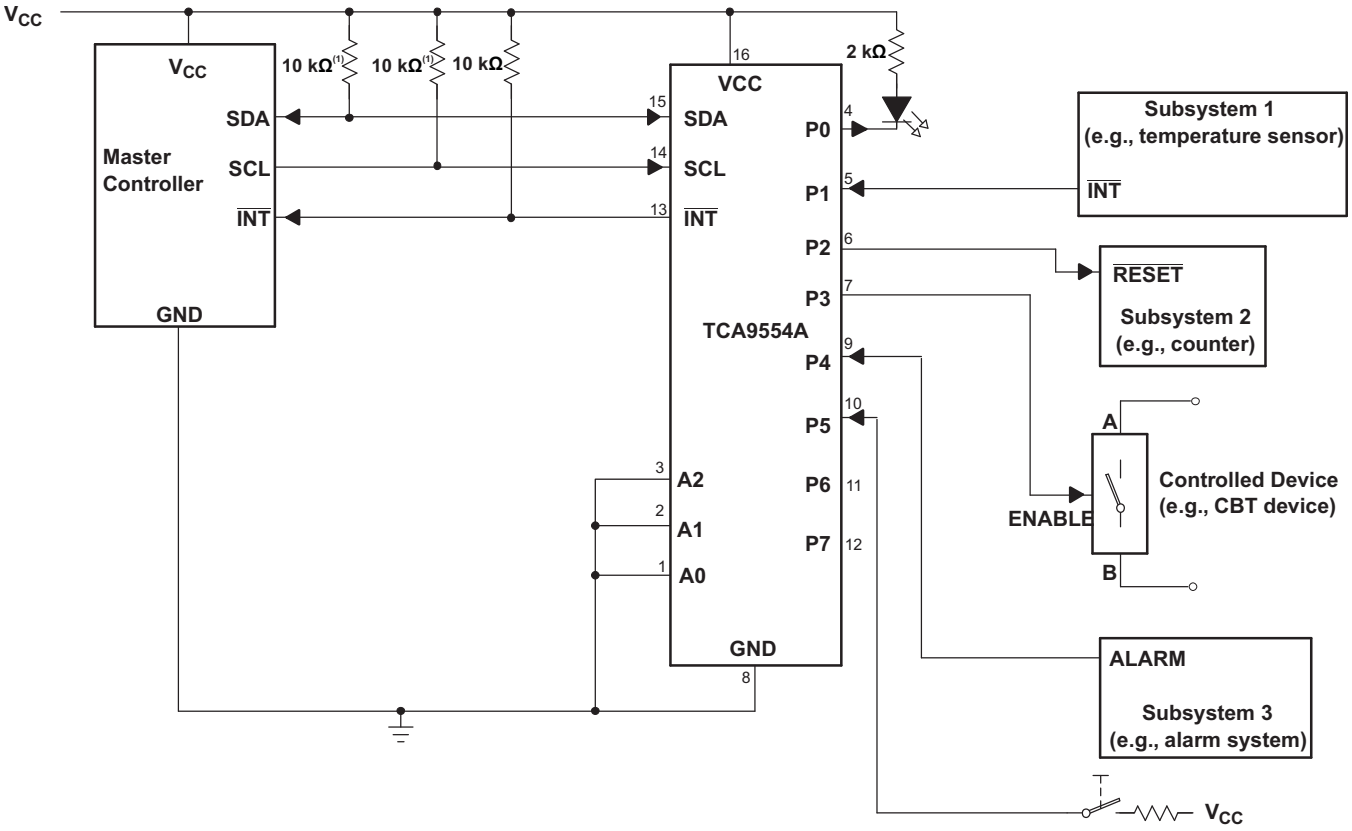
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Figure 24 shows an application in which the TCA9554A can be used.

10.2 Typical Application



(1) The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

A. Device address is configured as 0111000 for this example.

B. P0, P2, and P3 are configured as outputs.

C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and have internal 100-kΩ pullup resistors to protect them from floating.

Figure 24. Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

10.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 24. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 25 shows a high-value resistor in parallel with the LED. Figure 26 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

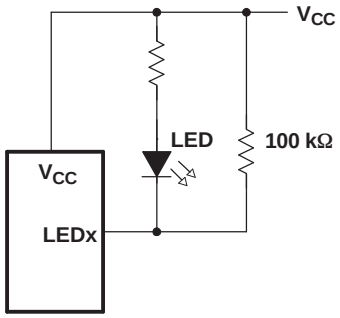


Figure 25. High-Value Resistor in Parallel With LED

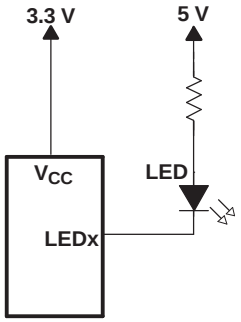


Figure 26. Device Supplied by a Lower Voltage

Typical Application (continued)

10.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

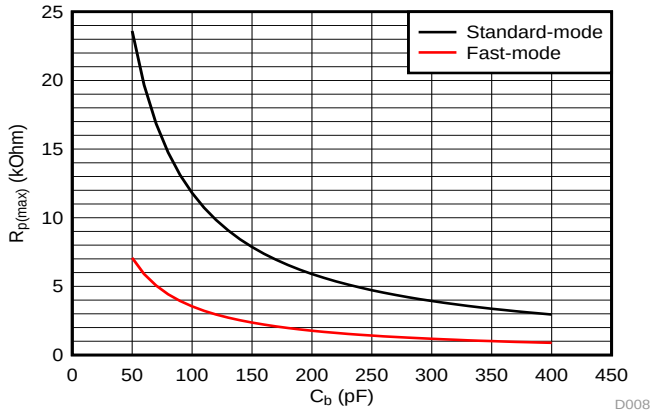
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9554A, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

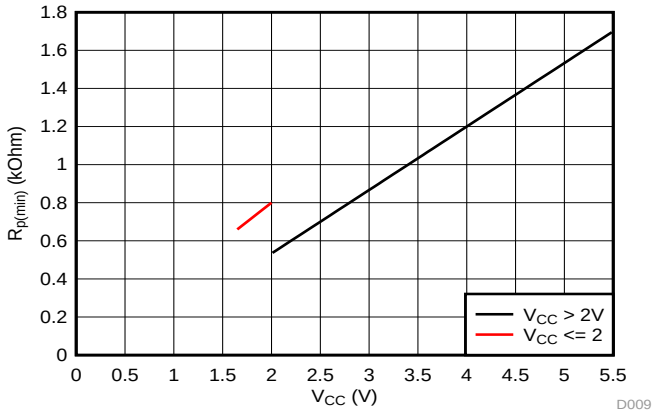
10.2.3 Application Curves



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 27. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 28. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

11 Power Supply Recommendations

11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9554A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and Figure 29.

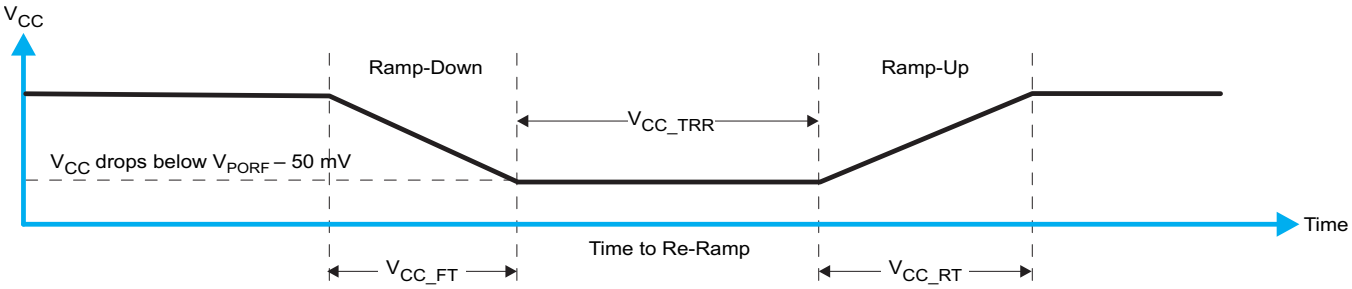


Figure 29. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 8 specifies the performance of the power-on reset feature for TCA9554A for both types of power-on reset.

Table 8. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 29	1			ms
V_{CC_RT}	Rise rate	See Figure 29	0.1			ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 29	2			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 30			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 30			10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 30 and Table 8 provide more information on how to measure these specifications.

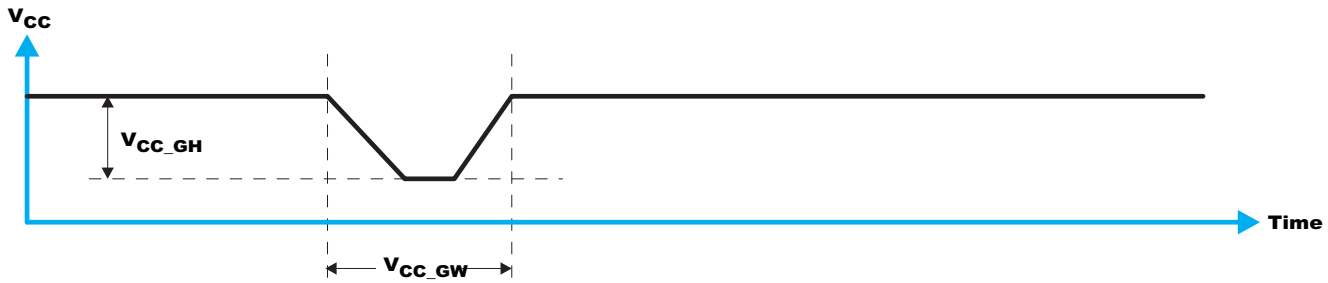


Figure 30. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 31 and Table 8 provide more details on this specification.

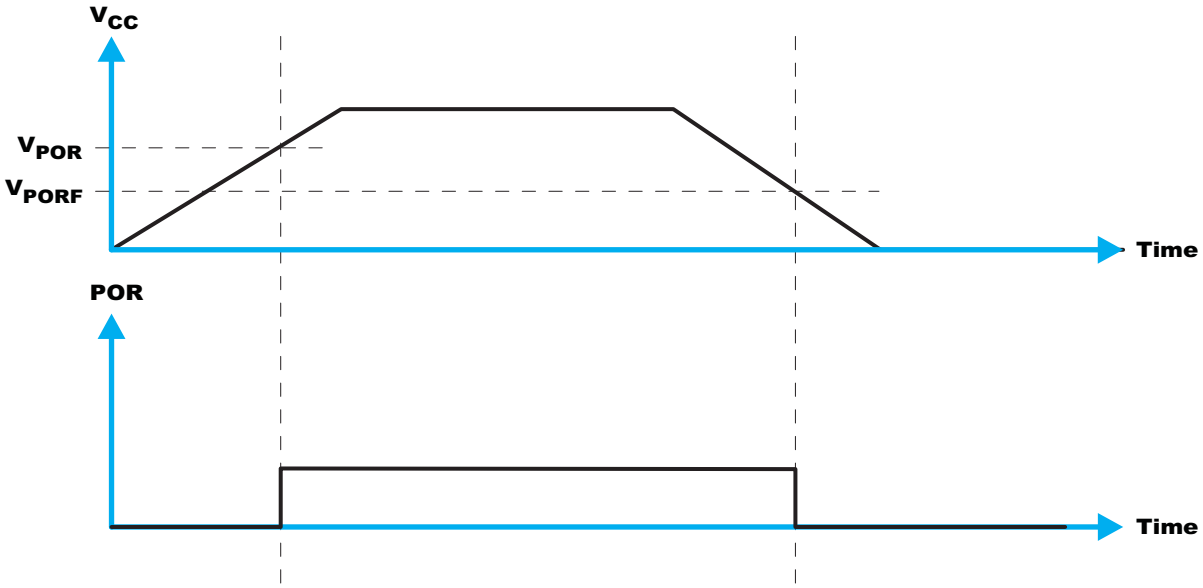


Figure 31. V_{POR}

12 Layout

12.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9554A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCA9554A as possible. These best practices are shown in Figure 32.

For the layout example provided in Figure 32, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 32.

12.2 Layout Example

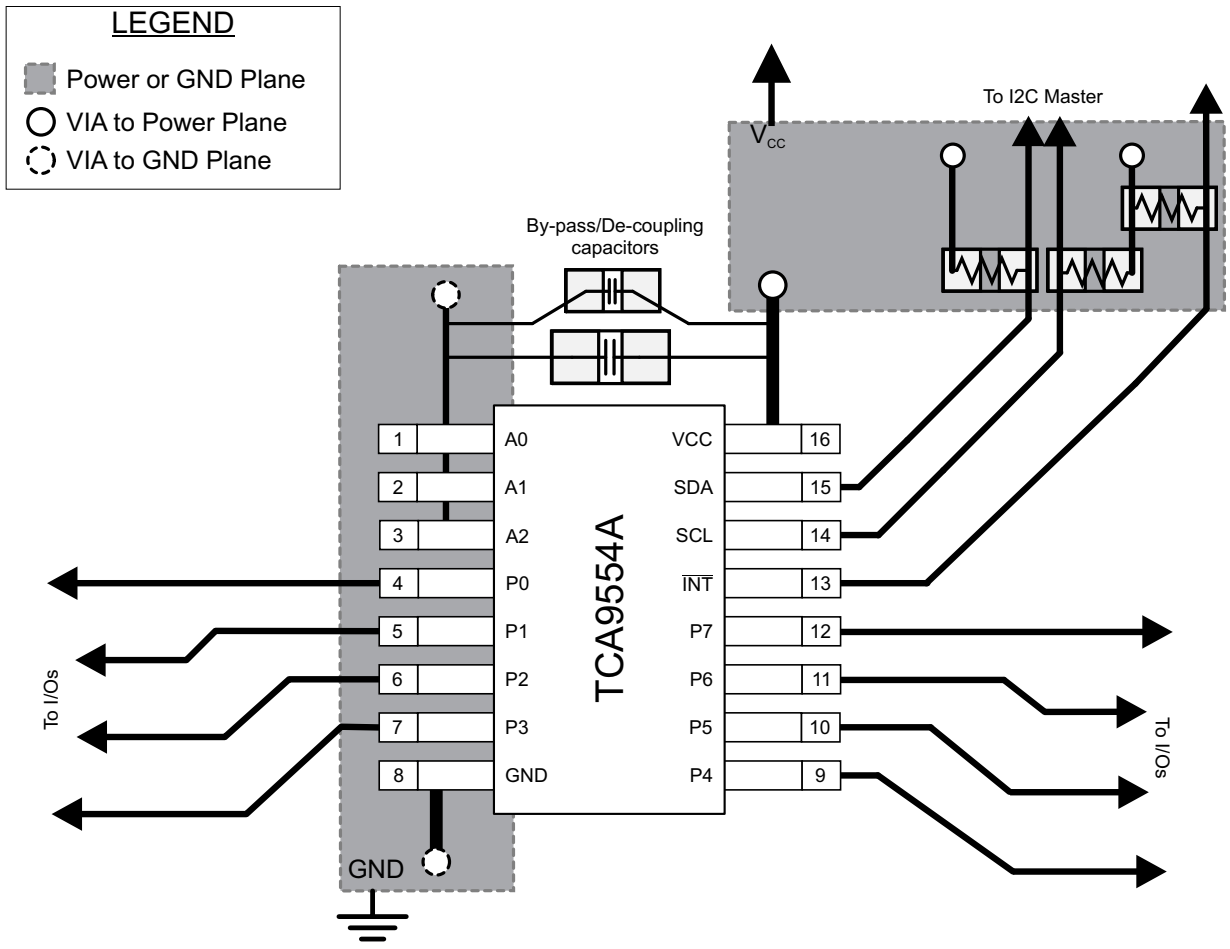


Figure 32. TCA9554A Layout

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9554APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW554A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

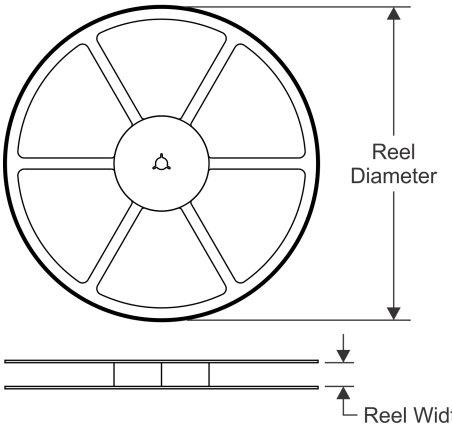
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

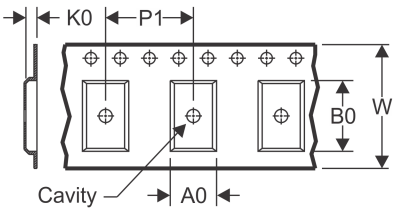
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

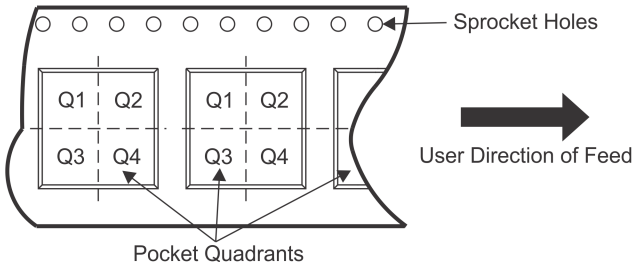


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

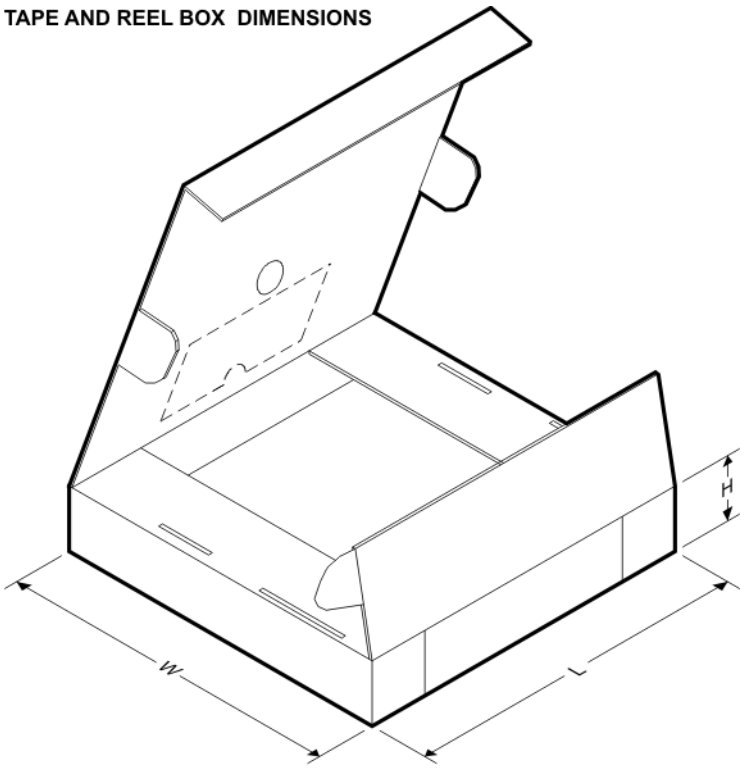
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9554APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

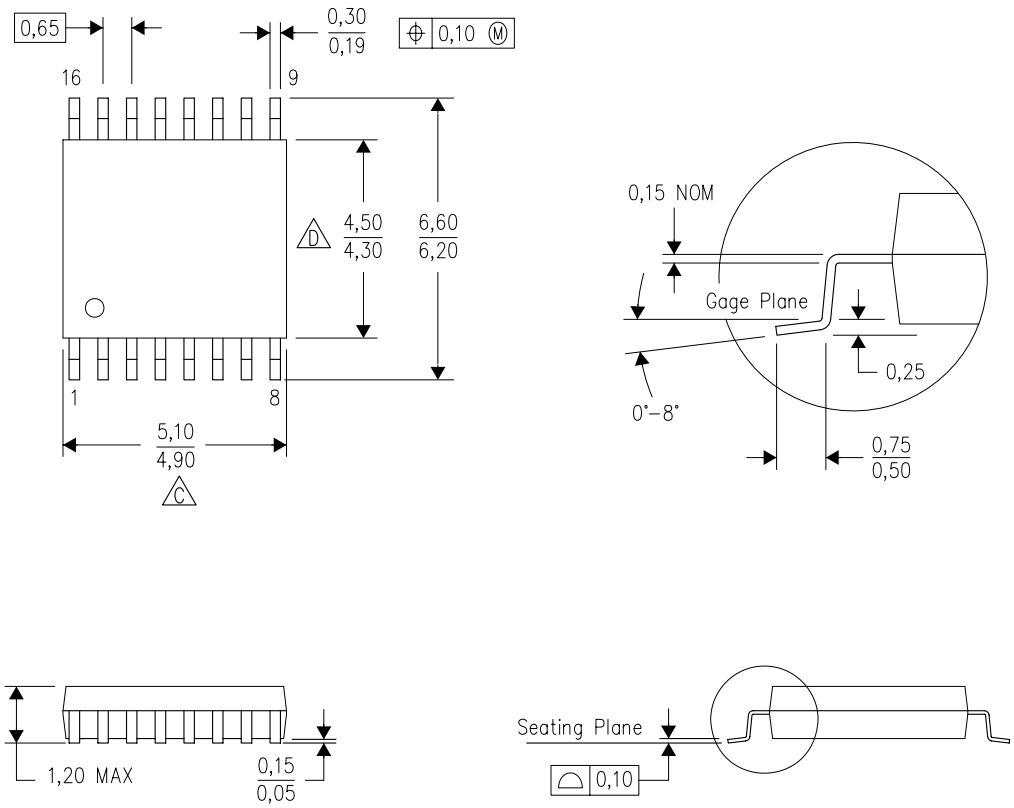
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9554APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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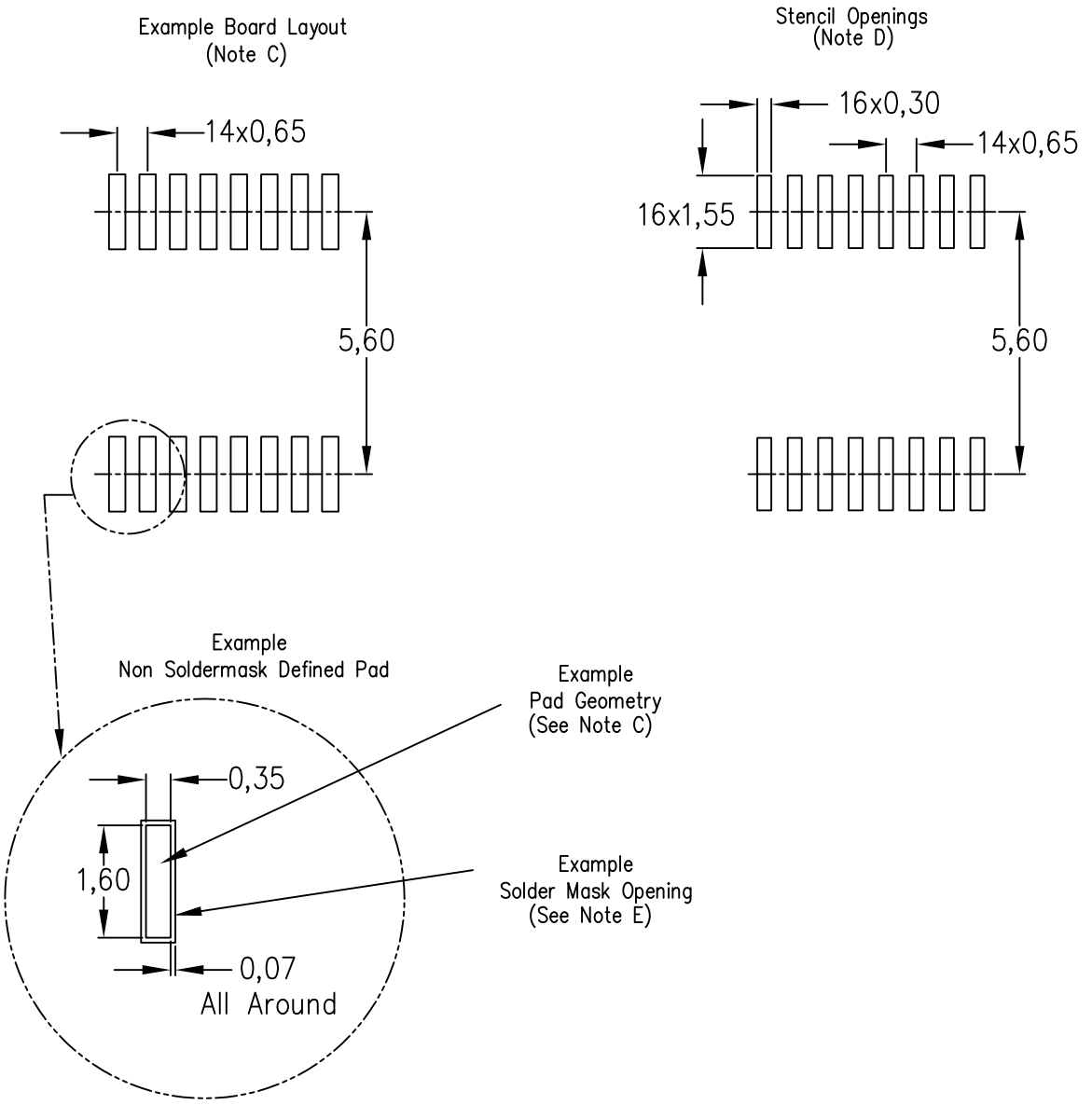
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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